



**i7050**  
**i7051**  
**200 Mbps Limiting Amplifiers**  
**Data Sheet**

**iCreate Technologies Corporation**

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# i7050

# i7051

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For more information please contact:

**iCreate Technologies Corporation**

No. 6, Technology Rd. V, Science-Based Industrial Park,  
Hsinchu, Taiwan 300, R.O.C.

Phone +886-3-579-0000

Fax +886-3-579-0077

e-mail [support@icreate.com.tw](mailto:support@icreate.com.tw)

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## +3.3V to +5.0V, 200Mbps Limiting Amplifiers

### 1. Introduction

#### 1.1. General description

The i7050/i7051 limiting amplifiers, with complementary PECL data outputs, are designed for fiber-optic based communication with data rate up to 200 Mbps.

Each device includes a programmable signal-level detector, allowing the user to set the threshold level at which PECL data outputs are enabled. The hysteresis is fixed internally in 2dB optical to prevent chattering when the signal level is close to the threshold level. The i7050's signal detect outputs are compatible with PECL-logic levels. The i7051 has CMOS signal detect outputs.

STB and JAM can be used to implement a squelch function, which gives fixed logic levels at data outputs when the input signal is below the programmed threshold level.

#### 1.2. Applications

- ✧ SDH/SONET/ATM
- ✧ Fast Ethernet
- ✧ FDDI
- ✧ ESCON

#### 1.3. Features

- ✧ Programmable chatter-free signal level detector.
- ✧ 1.6 mV input sensitivity (differential).
- ✧ 3.3V to 5V supply voltage.
- ✧ PECL data outputs.
- ✧ PECL signal detect logic interface (i7050).
- ✧ CMOS signal detect logic interface (i7051).
- ✧ Available in 16-pin QSOP and 20-pin TSSOP package.

### 2. Pin configuration and definition

#### 2.1. Pin configuration

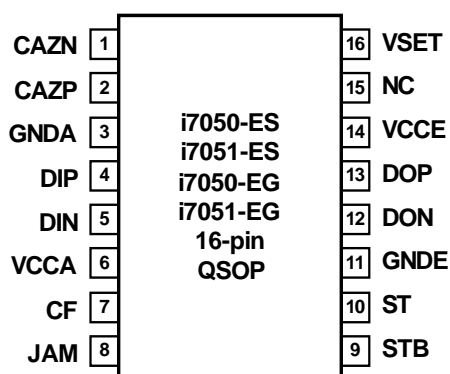


Figure 1. 16-pin QSOP configuration

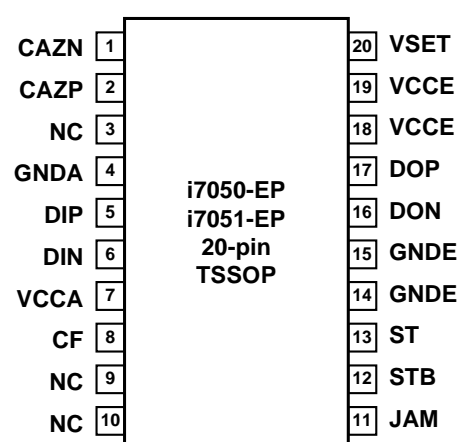


Figure 2. 20-pin TSSOP configuration

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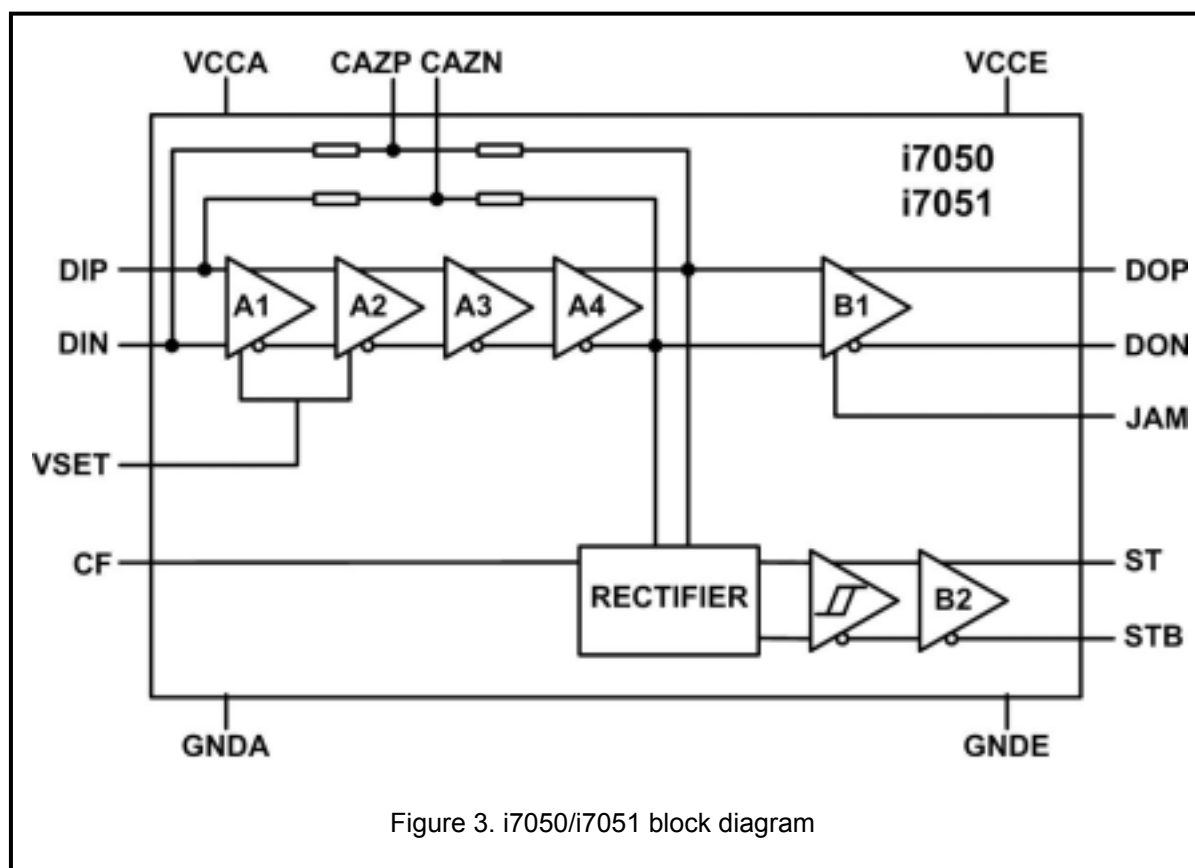
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## 2.2. Pin definition

Pin Name	16-pin QSOP Pin No.	20-pin TSSOP Pin No.	Function
CAZN	1	1	Auto-zero capacitor pin. Connect a capacitor between this pin and CAZP.
CAZP	2	2	Auto-zero capacitor pin. Connect a capacitor between this pin and CAZN.
GNDA	3	4	Analog ground pin. Connect to the most negative supply.
DIP	4	5	Differential data input. Complementary to pin DIN.
DIN	5	6	Differential data input. Complementary to pin DIP.
VCCA	6	7	Analog power supply pin. Connect to the most positive supply.
CF	7	8	Level-detect filter capacitor pin. Connect a capacitor between this pin and VCCA.
JAM	8	11	PECL/CMOS compatible input controlling output buffers DON and DOP.
STB	9	12	Input signal level detect status. STB is high when the input signal is below the threshold level set by the user. STB is compatible with PECL logic (i7050) or CMOS logic (i7051).
ST	10	13	PECL complement of STB (i7050). CMOS complement of STB (i7051).
GNDE	11	14,15	Digital ground pin. Connect to the most negative pin.
DON	12	16	PECL compatible data output. Complementary to DOP.
DOP	13	17	PECL compatible data output. Complementary to DON.
VCCE	14	18,19	Digital power supply pin. Connect to the most positive supply.
VSET	16	20	Input threshold-level setting circuit. Connect to analog ground via a resistor.
NC	15	3,9,10	Not connected.

### 3. Block diagram



## 4. Electrical specifications

### 4.1. Recommended operating conditions

PARAMETER	SYMBOL	RATING	UNITS
Power Supply	VCC	3.0 to 5.5	V
Operating Ambient	TA	-40 to 85	°C

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## 4.2. DC characteristics

(VCC=VCCA=VCCE=+3.0V to +5.5V, T<sub>A</sub>= -40 °C to 85 °C, unless otherwise noted. Typical values are at VCC=VCCA=VCCE=+3.3V, T<sub>A</sub>=+25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Signal Voltage	VIN	Single-ended:	0.8		500	mV
		Differential:	1.6		1000	
Equivalent Input Offset Voltage	VOS				50	μV
Input Level Detect Programmable Range	VTH	155 Mbps, 2 <sup>23</sup> -1PRBS	2		20	mV
Level Detect Hysteresis (optical)	VHYS	155 Mbps, 2 <sup>23</sup> -1PRBS		2		dB
PECL Output High	VOH	(Notes1, 2)	-1.02		-0.92	V
PECL Output Low	VOL	(Notes1, 2)	-1.72		-1.64	V
Supply Current	ICC	No ECL loads			35	mA

**Note1:** Outputs are terminated with 50 Ω to VCC-2V

**Note2:** Related to VCC

## 4.3. AC characteristics

(VCC=VCCA=VCCE=+3.0V to +5.5V, PECL outputs are terminated with 50 Ω to VCC-2V, T<sub>A</sub>= -40 °C to 85 °C, unless otherwise noted. Typical values are at VCC=VCCA=VCCE=+3.3V, T<sub>A</sub>=+25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bandwidth	BW		140			MHz
Input Resistance	RIN	Single-ended		10		KΩ
Input Capacitance	CIN				2	pF
Data Output Edge Speed	tR, tF	20% to 80%		700		ps
Pulse-Width Distortion	TPWD	(Notes3,4)		200		ps
Level Detect Time Constant	TLD		0.5	1	20	μs

**Note3:** TPWD = [(width of wider pulse)-(width of narrower pulse)] / 2

**Note4:** 155 Mbps, 1-0 pattern

#### 4.4. Typical operating characteristics

(PECL outputs are terminated with  $50\ \Omega$  to  $VCC-2V$ , input is a  $2^{23}$ -1PRBS pattern, 155Mbps,  $T_A = 25\ ^\circ C$ )

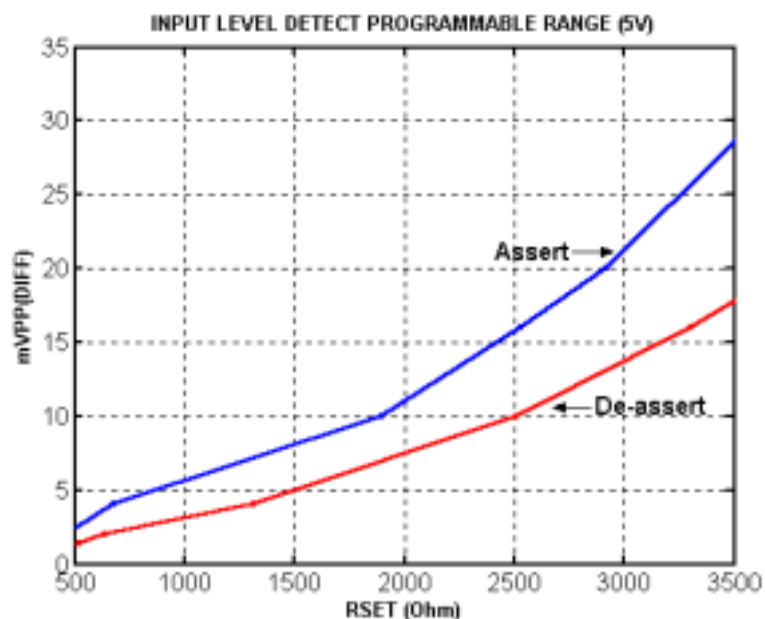


Figure 4. Level detect threshold voltage versus RSET (VCC=5V)

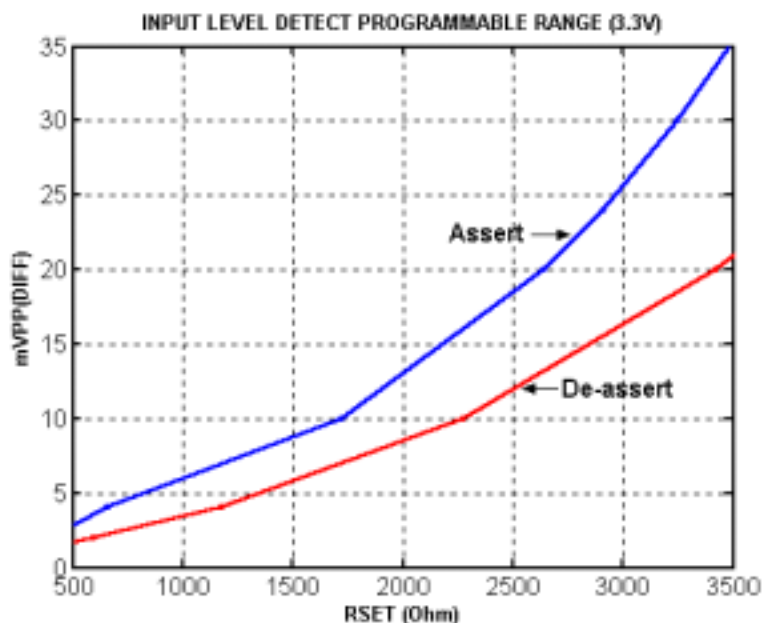


Figure 5. Level detect threshold voltage versus RSET (VCC=3.3V)

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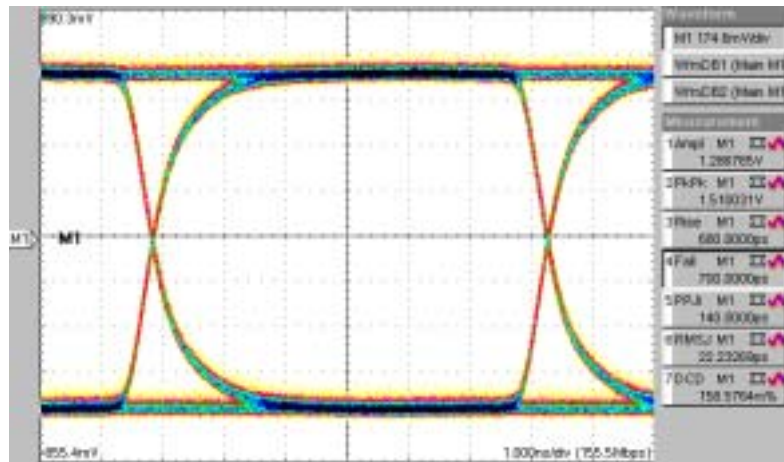


Figure 6. Differential outputs with 1000 mVpp differential inputs (VCC=3.3V)

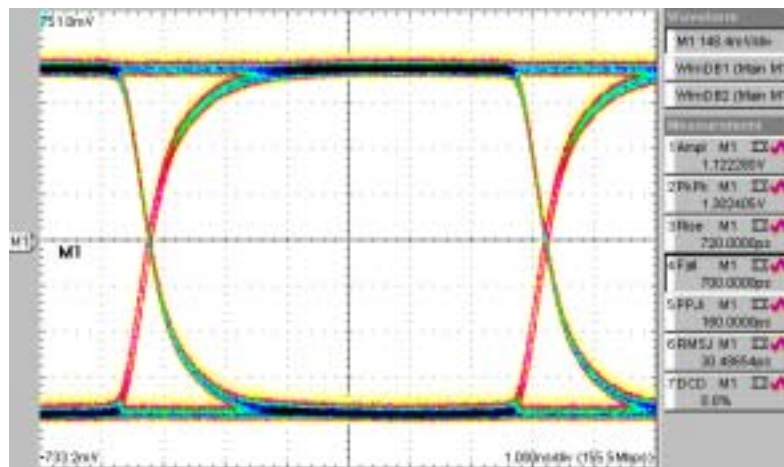


Figure 7. Differential outputs with 4 mVpp differential inputs (VCC=3.3V)

## 5. Product description

### 5.1. Input biasing

The input pins, DIP and DIN, are internally DC biased at approximately VCC-1V. The i7050/i7051 inputs are AC coupled via two external capacitors. These capacitors must be large enough to pass the lowest frequencies of

interest (consecutive identical digits). For 155Mbps SONET, 0.1 $\mu$ F coupling capacitors reacting with the input resistance will give a typical -3dB point of approximately 2.2 KHz.

## 5.2. DC offset compensation

A low-frequency feedback loop is integrated into i7050/i7051 to remove DC offset in the signal path. DC coupling inputs are not recommended, as this prevents the DC-offset-compensation from functioning normally.

An external capacitor (CAZ) between pins CAZP and CAZN, reacting with the input resistance, determines the offset-compensation circuit's time constant. CAZ is typically set to 10nF.

## 5.3. Signal level detection

Each device of the i7050/i7051 includes a programmable signal-level detector, allowing the user to set the threshold level at which PECL data outputs are enabled. The signal level can be set by using an external resistor (RSET). Please use the *typical operating characteristics* (figure 4. and figure 5.) to determine the RSET.

The time constant of the low-pass filter in level-detection circuitry can be controlled by using an external capacitor between pin CF and VCCA . 10nF is recommended to avoid false triggering. The hysteresis is fixed internally in 2dB optical. Note that RSET must be connected even if the level detect function is not required.

## 5.4. Squelch function

Connecting STB and JAM can implement a squelch function, which gives fixed logic levels at data outputs when the input signal is below the programmed threshold level. This prevents the outputs from reacting to noise in the absence of the input signal, and ensures that data will be received only when the signal is above the users' Bit-Error-Rate (BER) requirement.

## 5.5. PECL Output Termination

The i7050/i7051's termination technique is to terminate with a resistor equal to the impedance of the transmission line to a DC voltage of VCC-2V. Termination scheme and the values of termination resistors are given in figure 8 and figure 9.

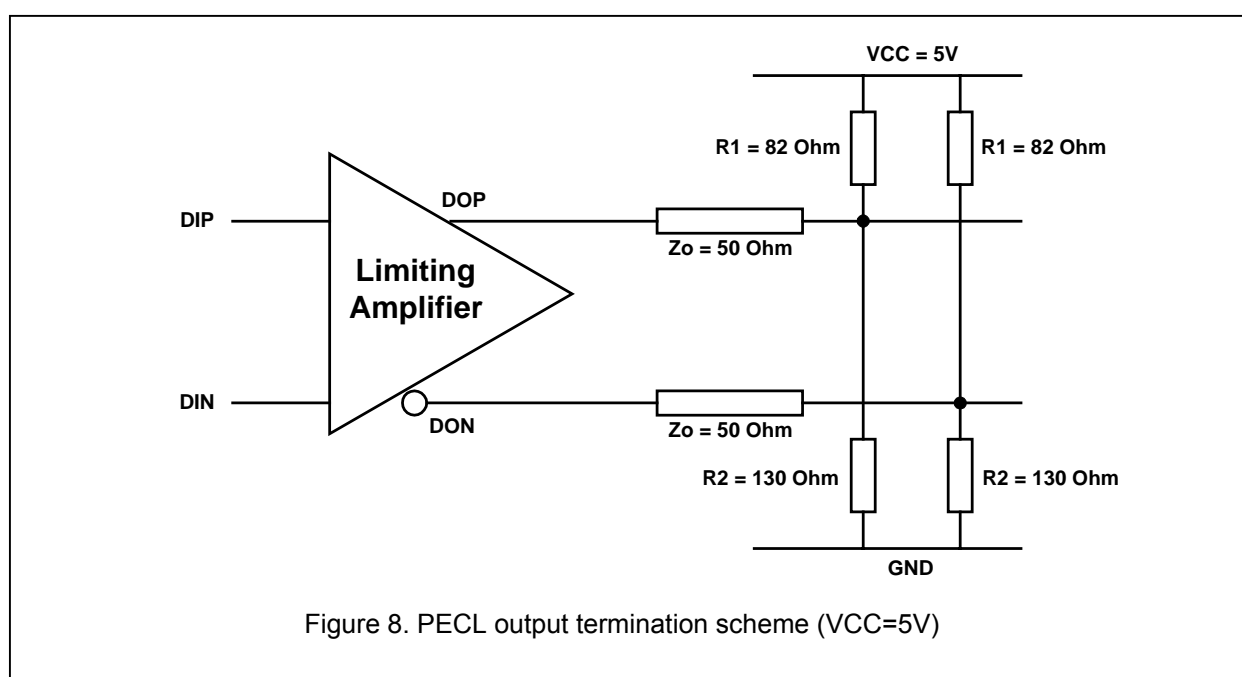
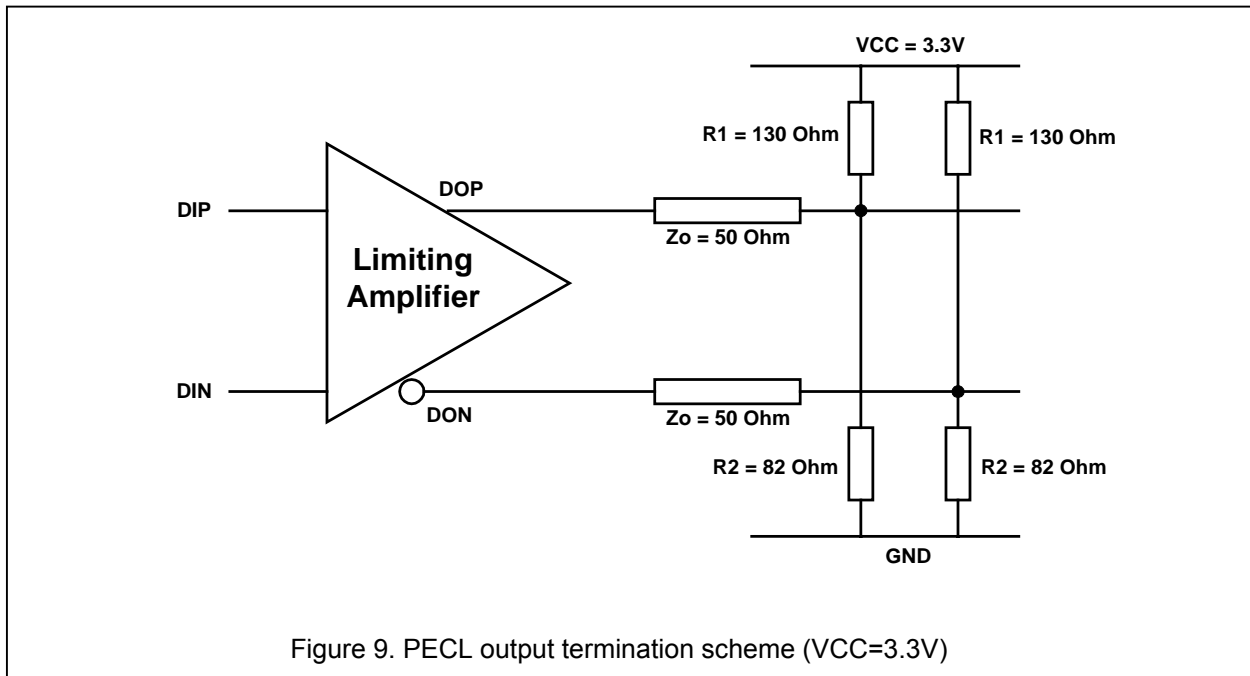


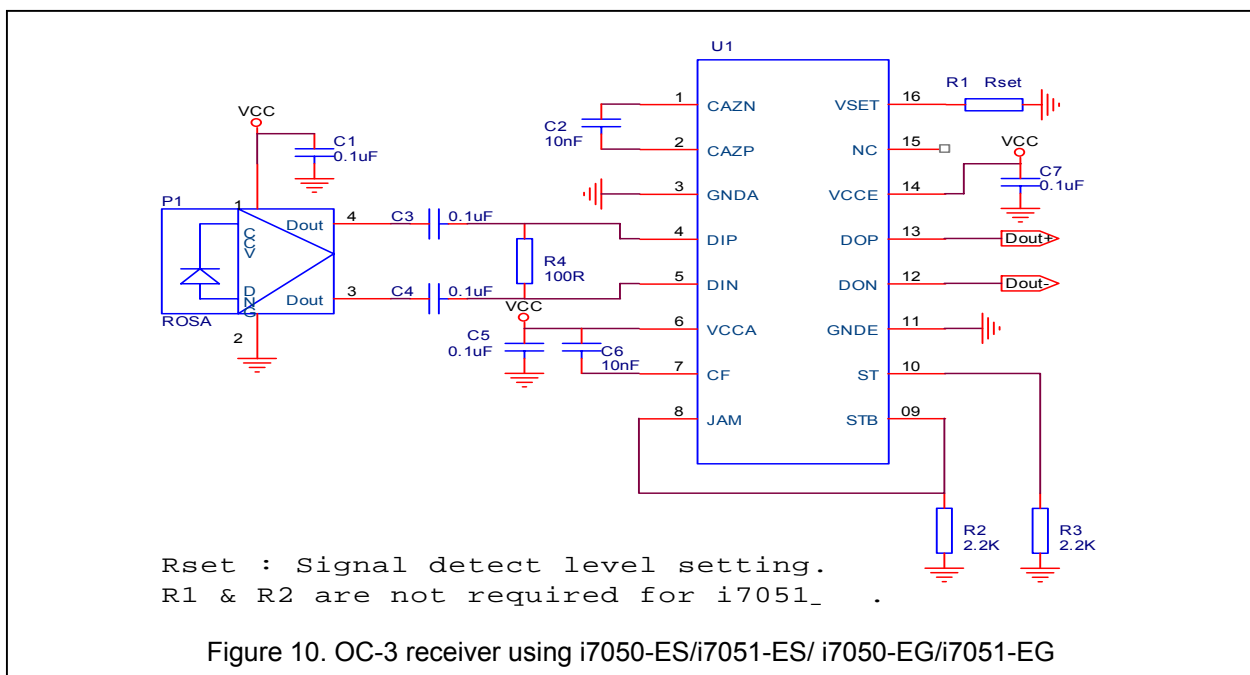
Figure 8. PECL output termination scheme (VCC=5V)

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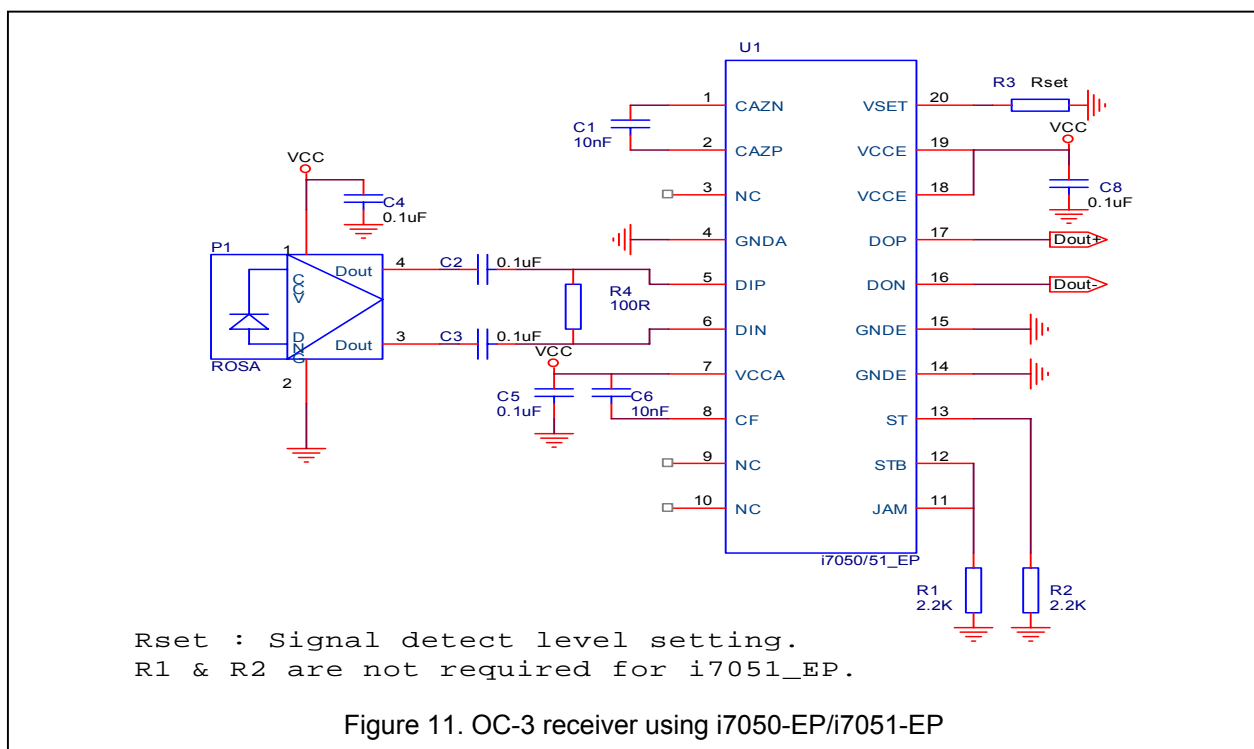


## 6. Typical application circuits

### 6.1. OC-3 receiver using i7050-ES/i7051-ES/ i7050-EG/i7051-EG



## 6.2. OC-3 receiver using i7050-EP/i7051-EP



## 7. Package outline

### 7.1. Package outline - 16-pin QSOP

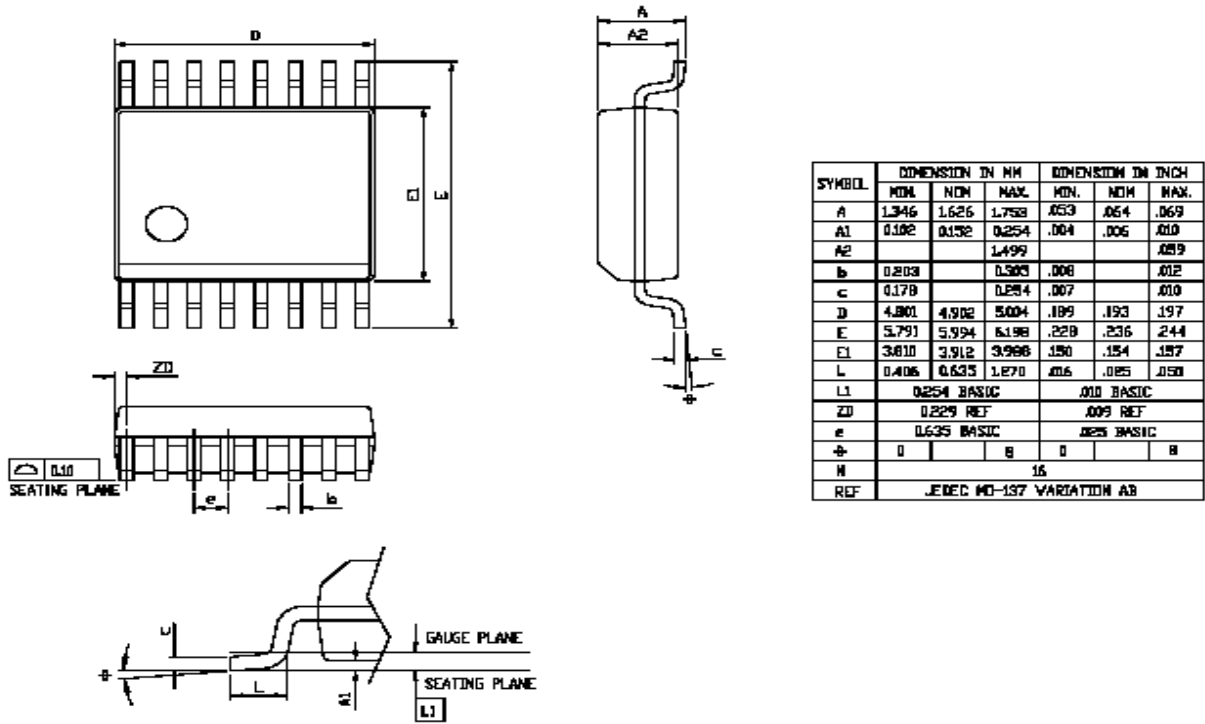


Figure 12. Package outline –16-pin QSOP

### 7.2. Package outline - 20-pin TSSOP

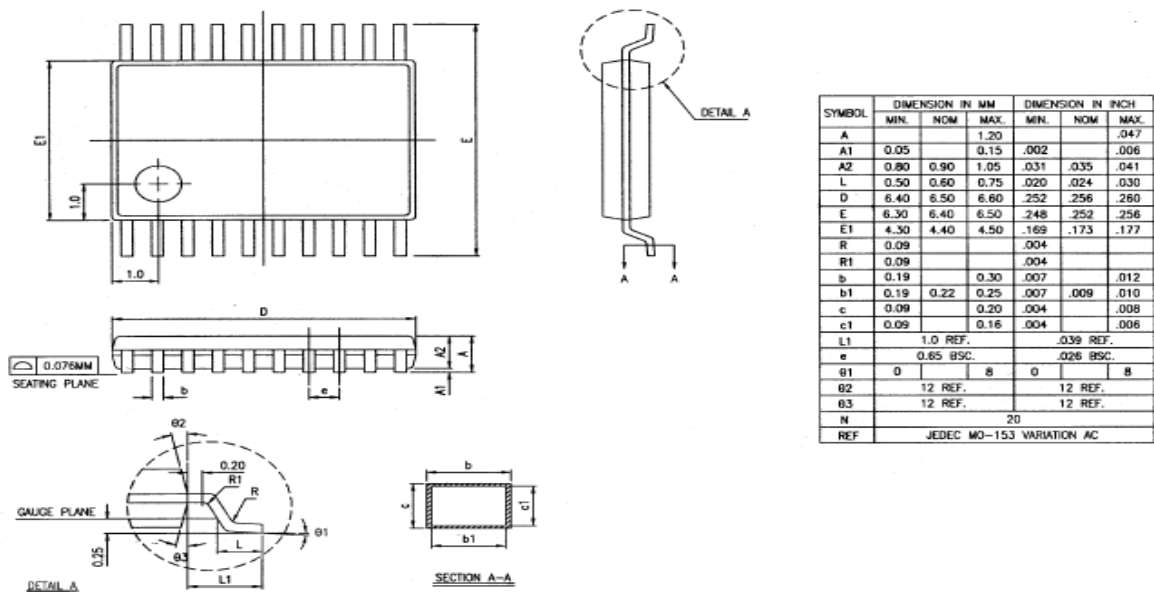


Figure 13. Package outline – 20-pin TSSOP

## 8. Ordering information

Part No.	Package
i7050-ES i7051-ES	16-pin QSOP
i7050-EP i7051-EP	20-pin TSSOP
i7050-EG i7051-EG	Green type 16-pin QSOP

### **iCreate Technologies Corporation**

No. 6, Technology Rd. V, Science-Based Industrial Park,  
Hsinchu, Taiwan 300, R.O.C.  
Tel: +886-3-579-0000 Fax: +886-3-579-0077