



Data Book

AU9368 USB Multi-LUN Flash Card Reader Controller Technical Reference Manual

Product Specification

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Product specification	This data sheet contains final product specifications.

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Feb 2005	1.17W/D27	Removed the schematics. Please contact our sales if you need it.
Jan 2005	1.18W/D27	Add "7.4 AC Electrical Characteristics" and modify "5.1 Pin Descriptions"



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1.0 Introduction

1.1. Description

The AU9368 is an integrated single chip memory card reader controller specially designed for notebook, hand-held and other PC peripheral devices, which require fewer components for small PCB area. It supports a widely used flash memory card such as CF, MD, SMC, xD Picture Card, MS, MS Pro, MS Duo, SD and MMC. It can be used as removable storage disks in enormous data exchange applications between PC and PC or PC and various consumer electronic appliances.

The AU9368 reads digital content saved on memory card that user captured with the portable device such as notebook, digital camera, MP3 player, PDA and mobile phone... etc. In addition, AU9368 allows user to transfer information such as data, graphics, texts or digital images from one electronic device to another quickly and easily. Furthermore, AU9368 integrates power switch function; manufacturers can use fewer components in their product design.

With AU9368, user's experience will be also further enhanced by the Plug-and-Play nature built into latest operation systems such as Windows 2000/XP and Mac OS X.

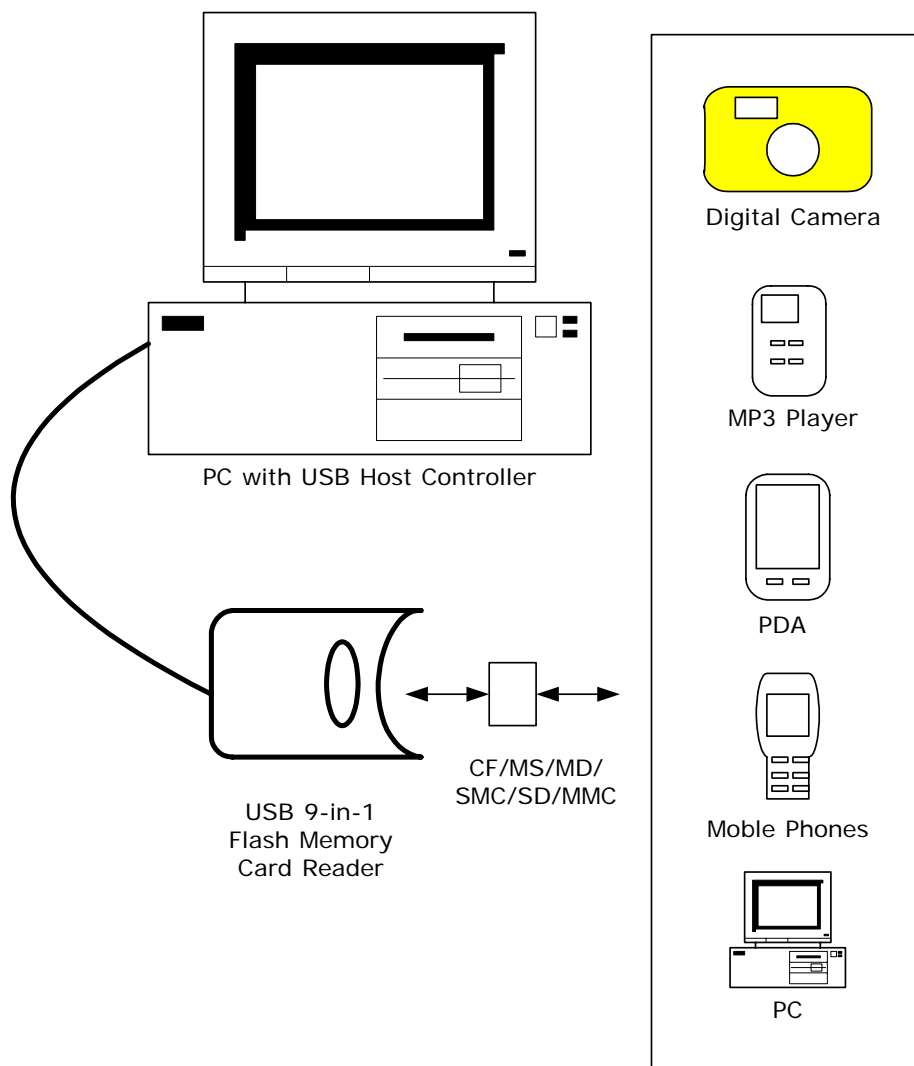
1.2. Feature

- Support USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport
- Support CF, SD, MS, MS PRQ, MS Duq, MS ROM Format, MMC, SMC, xD-Picture Card Format Specification and Microdrive device
- Work with default driver from Windows ME, Windows XP, Mac OS 9, and Mac OS X. Windows 98, Windows 2000 are supported by vendor driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer to 4GB to optimize performance
- Support optional external EEPROM for VID, PID and string customization
- Integrated power switch and power management circuit for each slot to reduce the BOM cost in PCB and meet USB power consumption requirement during suspend with card in the slot.
- CPU Runs at 30MHz, built-in 480MHz PLL
- Built-in 3.3V regulator
- 64-pin LQFP package
- Lead-free package available

2.0 Application Block Diagram

Following is the application diagram of a typical card reader product with AU9368. By connecting the card reader to a desktop or notebook PC through USB bus, AU9368 is implemented as a bus-powered, full speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

Figure 2.1 Au9368 Application Block Diagram





3.0 Operating Mode Selection

The Au9368 offers two operating modes. Mode 0 is used for CF/SD/SMC/MS/xD combo socket. While mode 1 is designed for single function socket. Mode 1 support xD card in a shared SMC socket.

Table 3.1 Mode definition table

Mode 0 (Modesel : 0)		Mode 1 (Modesel : 1)	
Slot 1	CF/SD/SMC/MS/xD	Slot 1	SD
		Slot 2	CF
		Slot 3	SMC/XD
		Slot 4	MS



4.0 Power Switch Feature

AU9368 integrates a 5V to 3.3V voltage regulator and power switch to replace all MOS chips for flash card power supply.

4.1. Card Power Output Current Range

- For MS/SD
 - ◆ MAX: 100mA

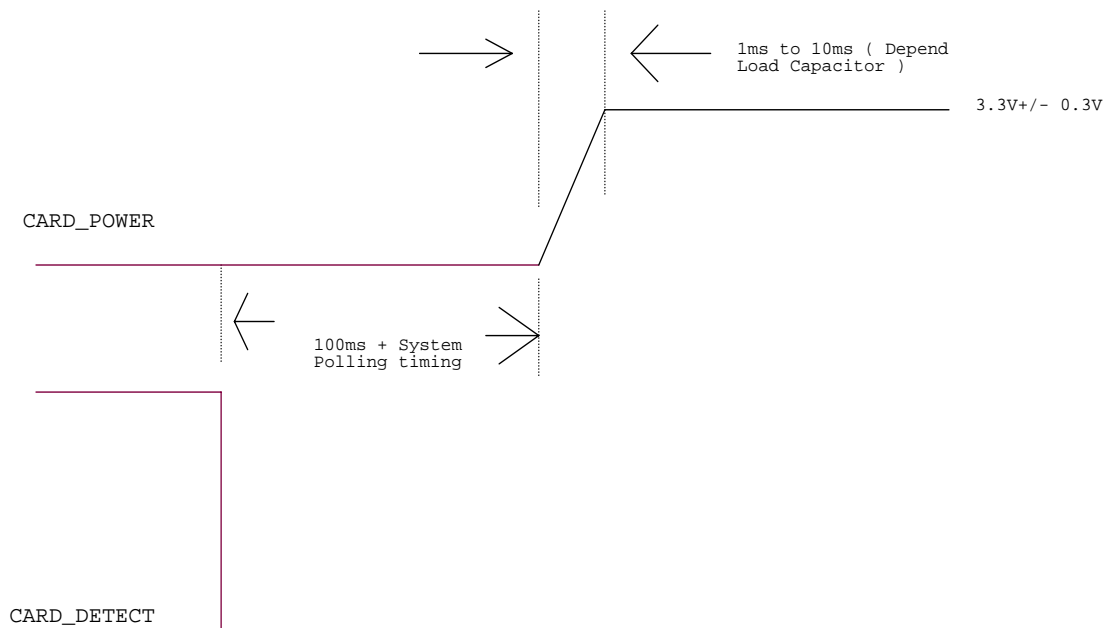
- For XD/SMC
 - ◆ MAX: 70mA

- For CF
 - ◆ MAX: 250mA

- Card power output voltage range
 - ◆ MS/XD/SD/SMC/CF: $3.3V \pm 0.3V$

- AU9368 will turn off all of Card Power in suspend mode

4.2. Card Detect Power-on Timing





5.0 Pin Assignment

The AU9368 is packed in 64-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

Figure 5.1 Pin Assignment Diagram

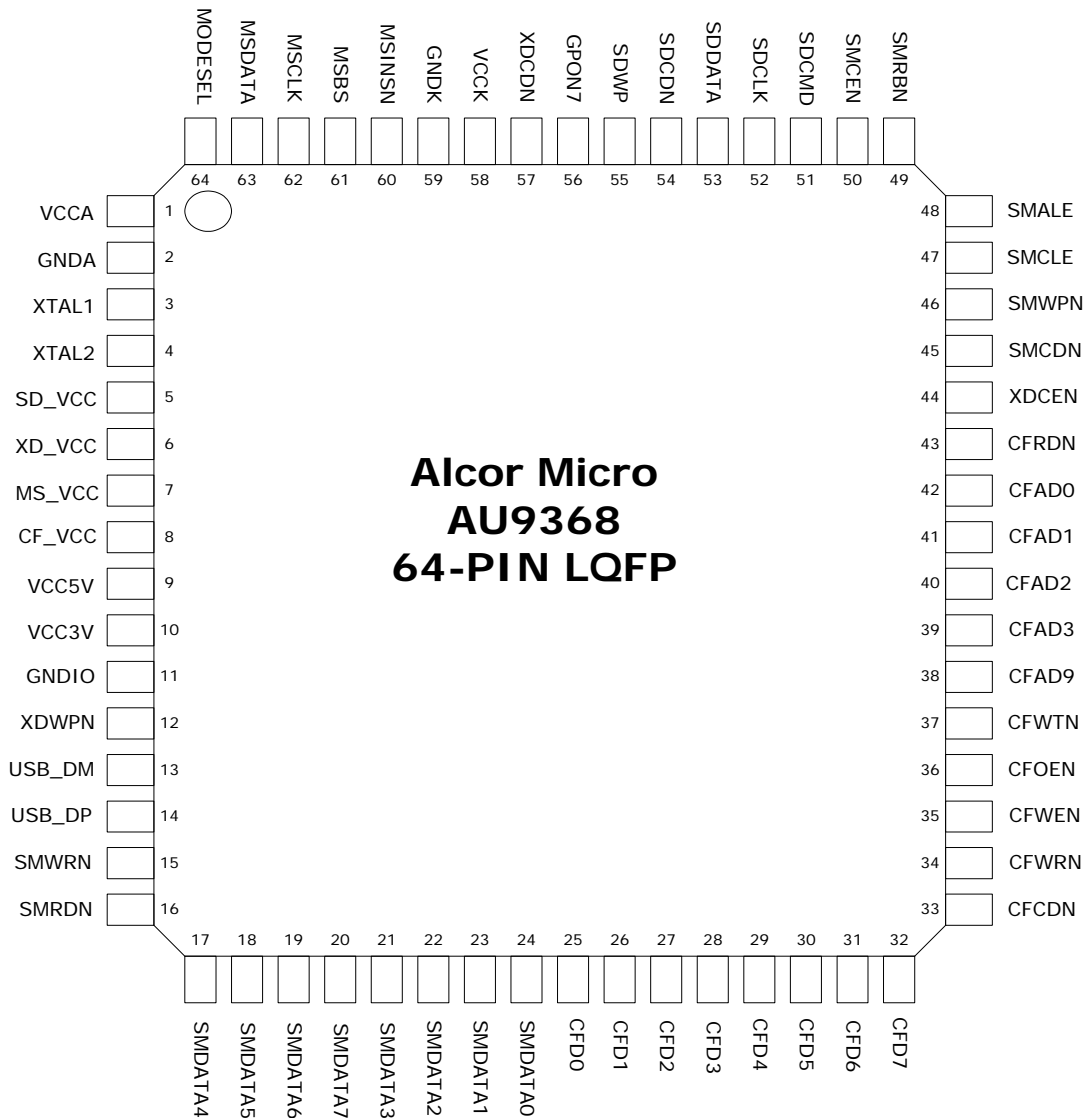




Table 5.1 Pin Descriptions

Pin	Pin Name	I/O Type	Description
1	VCCA	PWR	Analog 3.3V input
2	GND A	PWR	Analog GND
3	XTAL1	I	Crystal Oscillator input (12MHz)
4	XTAL2	O	Crystal Oscillator output (12MHz)
5	SD_VCC	PWR	SD card power
6	XD_VCC	PWR	SMC/XD power
7	MS_VCC	PWR	MS card power
8	CF_VCC	PWR	CF card power
9	VCC5V	PWR	VCC 5V power supply from USB
10	VCC3V	PWR	VCC 3.3V
11	GNDIO	PWR	PAD GND
12	XDWP N	O	XD write protect
13	USB_DM	I/O	USB DM
14	USB_DP	I/O	USB DP
15	SMWRN	O	SMC Write Enable
16	SMRD N	O	SMC Read Enable
17	SMDATA4	I/O	SMC DATA4
18	SMDATA5	I/O	SMC DATA5
19	SMDATA6	I/O	SMC DATA6
20	SMDATA7	I/O	SMC DATA7
21	SMDATA3	I/O	SMC DATA3
22	SMDATA2	I/O	SMC DATA2
23	SMDATA1	I/O	SMC DATA1
24	SMDATA0	I/O	SMC DATA0
25	CFD0	I/O	CF card data0
26	CFD1	I/O	CF card data1
27	CFD2	I/O	CF card data2
28	CFD3	I/O	CF card data3
29	CFD4	I/O	CF card data4
30	CFD5	I/O	CF card data5
31	CFD6	I/O	CF card data6
32	CFD7	I/O	CF card data7
33	CFCD N	I	CF card detect
34	CFWRN	O	CF card IOWR
35	CFWEN	O	CF card WE
36	CFOEN	O	CF card OE
37	CFWTN	I	CF card WAIT
38	CFAD9	O	CF card addr09
39	CFAD3	O	CF card addr03
40	CFAD2	O	CF card addr02
41	CFAD1	O	CF card addr01
42	CFAD0	O	CF card addr00
43	CFRD N	O	CF card IORD
44	XDCEN	O	XD card enable
45	SMCD N	I	SMC card detect
46	SMWP N	I	SMC write protect
47	SMCLE	O	SMC command latch enable

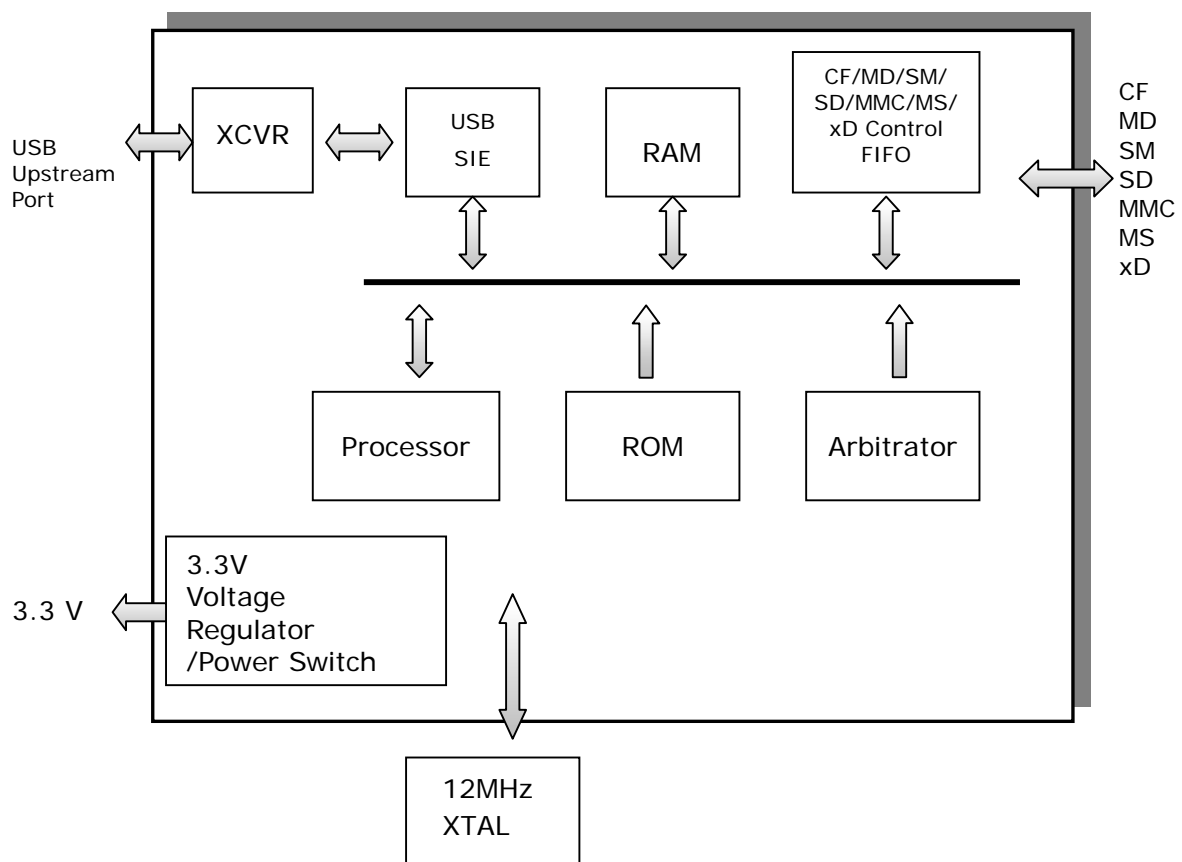


48	SMALE	O	SMC address latch enable
49	SMRBN	I	SMC Ready/Busy
50	SMCEN	O	SMCEN
51	SDCMD	I/O	SD CMD
52	SDCLK	O	SD CLK
53	SDDATA	I/O	SD DAT
54	SDCDN	I	SD card detect
55	SDWP	I	SD write protect
56	GPON7	I/O	LED for GPON7
57	XDCDN	I	XD card detect
58	VCKK	PWR	Core 3.3V VCC
59	GNDK	PWR	Core Ground
60	MSINSN	I	MS card INS.
61	MSBS	O	MS card BS
62	MSCLK	O	MS card CLK
63	MSDATA	I/O	MS card SDIO
64	MODESEL	I	Mode selection. ("0": 1 slot mode; "1": 4.5 slots mode)

6.0 System Architecture and Reference Design

6.1. AU9368 Block Diagram

Figure 6.1 AU9368 Block Diagram





7.0 Electrical Characteristics

7.1. Recommended Operating Conditions

Table 7.1 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CC}	Power Supply	4.75	5	5.25	V
V _{IN}	Input Voltage	0		V _{CC}	V
T _{OPR}	Operating Temperature	0		85	°C
T _{STG}	Storage Temperature	-40		125	°C

7.2. General DC Characteristics

Table 7.2 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I _{IL}	Input low current	no pull-up or pull-down	-1		1	μA
I _{IH}	Input high current	no pull-up or pull-down	-1		1	μA
I _{OZ}	Tri-state leakage current		-10		10	μA
C _{IN}	Input capacitance			5		ρF
C _{OUT}	Output capacitance			5		ρF
C _{BID}	Bi-directional buffer capacitance			5		ρF

7.3. DC Electrical Characteristics for 3.3 volts operation

Table 7.3 DC Electrical Characteristics for 3.3 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IL}	Input Low Voltage	CMOS			0.9	V
V _{IH}	Input High Voltage	CMOS	2.3			V
V _{OL}	Output low voltage	I _{OL} =4mA, 16mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =4mA, 16mA	2.4			V
R _I	Input Pull-up/down resistance	V _{il} =0V or V _{Ih} =V _{CC}		10K/200K		KΩ



7.4 AC Electrical Characteristics

GND=0V, $t_r = t_f = 3.0$ ns; $C_L = 50$ pF; $R_L = 500$ Ohms

Table 7.4 AC Electrical Characteristics

SYMBOL	PARAMETER	WAVEFORM	LIMITS (T_{AMB})					UNIT
			0° C to +25° C			0° C to +70° C		
			MIN	TYP	MAX	MIN	MAX	
tpLH tpHL	VMO/VPO to D+/D- Full Speed	1	0 0		12 12	0 0	14 14	ns
trise tfall	Rise and Fall Times Full Speed	2	4 4	9 9	20 20	4 4	20 20	ns
tRFM	Rise and Fall Time Matching Full Speed		90		110	90	110	%
tpLH tpHL	VMO/VPO to D+/D- Low Speed	1		120 120	300 300		300 300	ns
trise tfall	Rise and Fall Times Low Speed	2	75 75		300 200	75 75	300 200	ns
tRFM	Rise and Fall Time Matching Low Speed		70		130	70	130	%
tpLH tpHL	D+/D- to RCV	3		9 9	16 16		16 16	ns
tpLH tpHL	D+/D- to VP/VM	1		4 4	8 8		8 8	ns
tpHZ tpZH tpLZ tpZL	OE# to D+/D- $R_L =$ 500ohm	4			12 12 10 10		12 12 10 10	ns
tsu	Setup for SPEED	5	0					ns
Vcr	Crossover point ¹	3	1.3		2.0	1.3	2.0	V

NOTES:

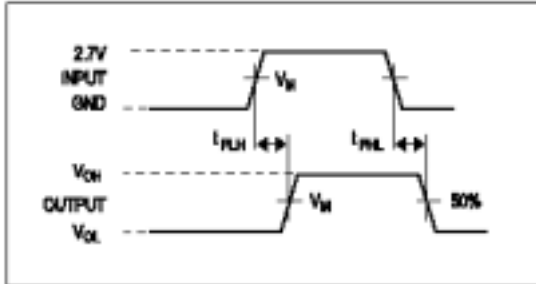
1. The crossover point is in the range of 1.3V to 2.5V for the low speed mode with a 50 pF capacitance.



Figure 7.1 Electrical Characteristics Diagram

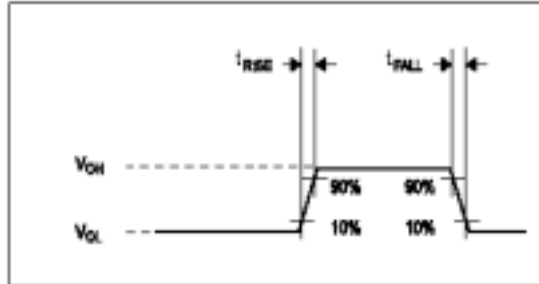
AC WAVEFORM 1.

D+/D- TO VP/VM OR VPQ/VMQ TO D+/D-



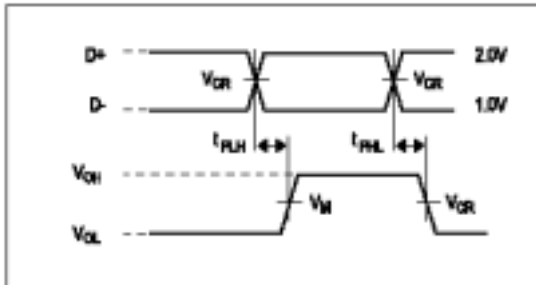
AC WAVEFORM 2.

RISE AND FALL TIMES



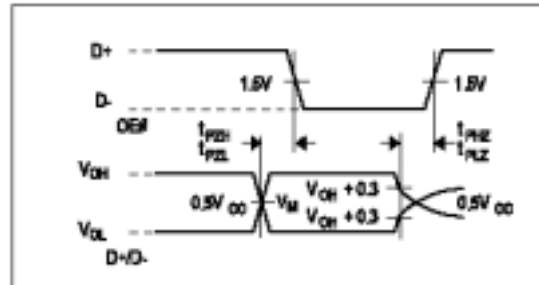
AC WAVEFORM 3.

D+/D- TO RCV



AC WAVEFORM 4.

OE# TO D+/D-



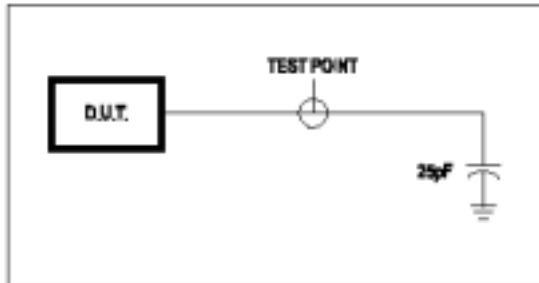
AC WAVEFORM 5.

SETUP FOR SPEED



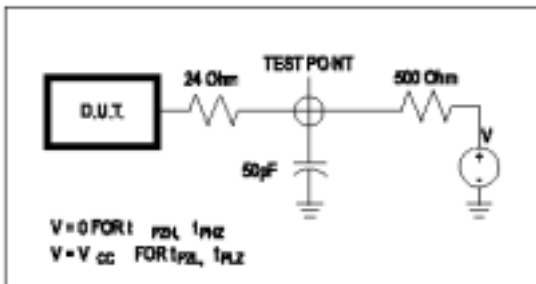
TEST CIRCUIT 1.

LOAD FOR VM/VP AND RCV



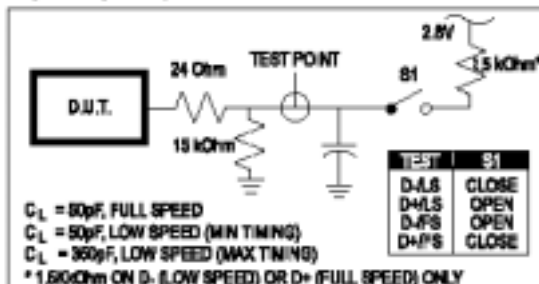
TEST CIRCUIT 2.

LOAD FOR ENABLE AND DISABLE TIMES



TEST CIRCUIT 3.

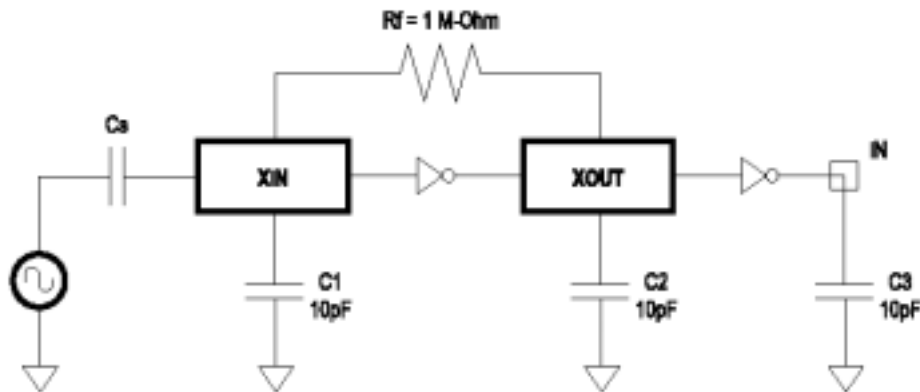
LOAD FOR D+/D-



7.5 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, C_s , is much larger than C_1 and C_2 .

Figure 7.2 Crystal Oscillator Circuit Setup for Characterization



7.6 ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body-Model (HBM) and Machine-Model (MM), according to MIL-STD 883 and EIAJ IC-121 respectively.

- Human-Body-Model stresses devices by sudden application of a high voltage supplied by a 100pF capacitor through 1.5k-ohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200pF capacitor through very low (0 ohm) resistance.

Test circuit & condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

Table 7.5 ESD Data

Model	Mode	S/S	Target	Results
HBM	Vdd, Vss, I/C	15	6000V	PASS
MM	Vdd, Vss, I/C	15	200V	PASS

7.7 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5Volts and ground respectively.

Testing was started at 5.0V (Positive) or 0V (Negative), and the DUT was biased for 0.5 seconds.

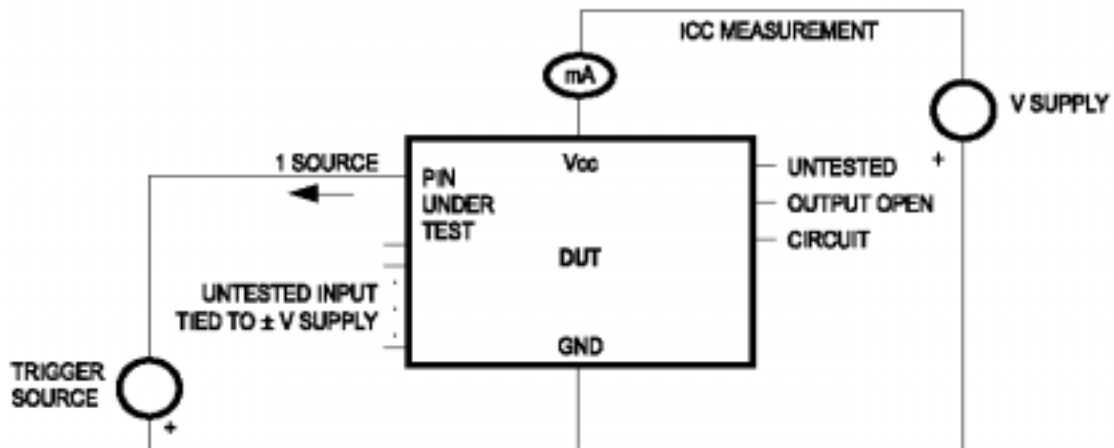
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=00mA, Icc=100mA), then the voltage was increased by 0.1Volts and the pin was tested again.

The JEDEC JC-40.2 CMOS Logic standardization committee recommended this procedure.

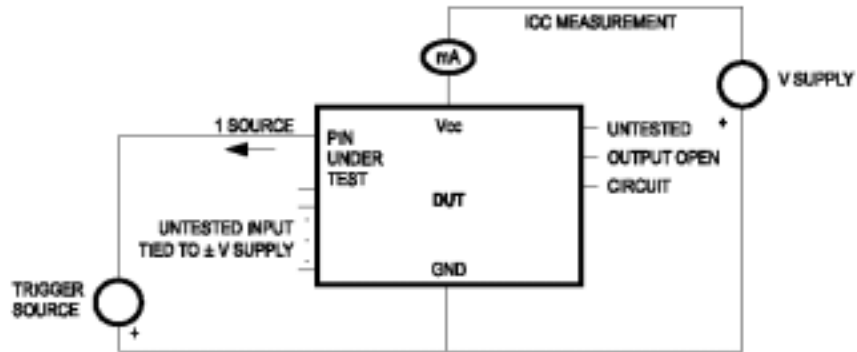
Notes:

1. DUT: The device under test.
2. PUT: The pin under test.

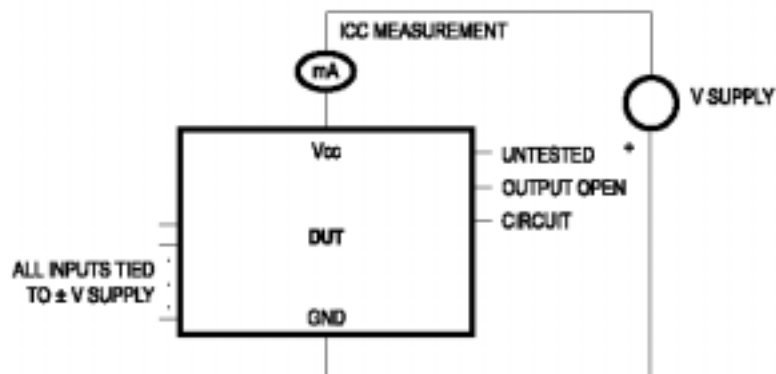
Figure 7.3 Latch-Up Test Results



Test Circuit: Positive Input/Output Overvoltage/Overcurrent



Test Circuit: Negative Input/Output Overvoltage/Overcurrent



Supply Overvoltage Test

Table 7.6 Latch-Up Data

Mode		Voltage (V)/Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0	5	Pass
Current	+	200	5	Pass
	-	200	5	Pass
Vdd - Vxx		9.0	5	Pass

8.0 Mechanical Information

Δ NOTES : DIMENSIONS * D1 * AND * E1 * DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE * D1 * AND * E1 * ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.05	1.80	0.083	0.002	0.071	0.003
A1	1.35	1.40	0.053	0.053	0.055	0.057
A2	0.17	0.20	0.007	0.008	0.009	0.009
b	0.09	0.15	0.004	0.004	0.006	0.006
c	0.50	0.50	0.020	0.020	0.020	0.020
D	12.00	12.00	0.472	0.472	0.472	0.472
D1	10.00	10.00	0.394	0.394	0.394	0.394
E	12.00	12.00	0.472	0.472	0.472	0.472
E1	10.00	10.00	0.394	0.394	0.394	0.394
L	0.45	0.60	0.018	0.024	0.024	0.030
L1	1.00	REF.	0.039	REF.	0.039	REF.
R1	0.08		0.003		0.003	
R	0.08	0.20	0.003	0.008	0.008	0.008
φ	0	3.5	7	0	3.5	7
φ1	0		0			
φ2	11	12	13	11	12	13
φ3	11	12	13	11	12	13

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REV.	DESCRIPTION	BY	DATE
ORIG.	DRAWING ISSUE	SANDY CHEN	98.11.26
A	ADD NOTES	SANDY CHEN	00.01.21

CWT Chant World Technology Inc.		<input type="checkbox"/> ANGLAR ± T <input type="checkbox"/> FINISH <input type="checkbox"/> HESS <input type="checkbox"/> SCALE
TITLE	LOPP BAL PACKAGE OUTLINE	UNIT
BODY SIZE	10 x 10 MM	QTY
DESIGNED	Jason Chung 98.11.26	FILE NAME
CHECKED	C.C.CHIO 00.01.26	DWG. NO.:
APPROVED	C.C.CHIO 00.01.26	PG-008B



9.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

PCB	Printed Circuit Board
BOM	Bill of Material
SIE	Serial Interface Engine
CF	Compact Flash
MD	Micro Drive
SMC	SmartMedia Card
MS	Memory Stick
SD	Secure Digital
MMC	Multimedia Card



【MEMO】

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