



# Data Book

**AU6369**

**USB 2.0 Single-Slot SD/MS/xD  
Flash Memory Card Reader  
Technical Reference Manual**

**Product Specification**

**Official Release**

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## Data sheet status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

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May 2005	2.02W/A31	Removed the schematics. Please contact our sales if you need it.



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# 1.0 Introduction

## 1.1 Description

The AU6369 is a highly integrated single chip for USB SD/MS/xD card reader controller. It supports USB v2.0 high-speed transmission to the entire popular storage media interface on one chip, such as, Secure Digital (SD), Multi Media Card (MMC), Memory Stick (MS, MS Pro, MS Duo), Digital photo (xD) and Smart Media Card (SMC).

The AU6369 supports USB v2.0 and USB v1.0 Storage Class specification. It can read digital contents stored on memory card designed to cover a wide area of applications such as digital cameras, PDAs, MP3 players and smart phones...etc. With the AU6369, users can transfer digital data between flash memory card and PC or these electronic devices.

The integration of various mixed mode makes component AU6369 is the most powerful and most effective solution for single-slot flash memory reader.

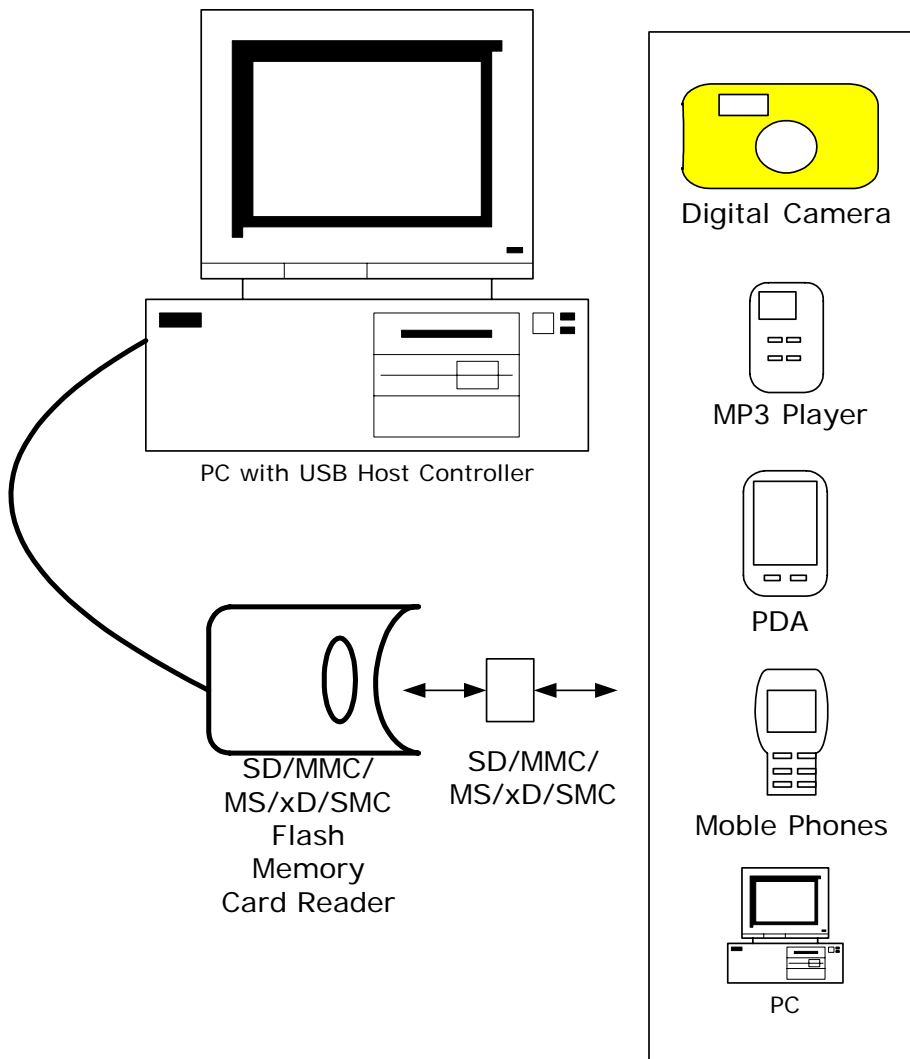
## 1.2 Features

- Support USB v2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial interface Engine
- Support SD/MMC ,xD/SMC and MS/MS PRO/MS ROM/MS Duo specification
- Work with default driver from Windows ME, Windows XP, and Mac OS X. Windows 98, Windows 2000 are supported by vendor AP from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer optimize performance
- Support auto-detecting slot with card inserted on Win 2000 without driver.
- Support LED for bus activity indication.
- CPU Runs at 30MHz, built-in 480MHz PLL

## 2.0 Application Block Diagram

Following is the application diagram of a typical card reader product with AU6369. By connecting the card reader to a desktop or notebook PC through USB bus, AU6369 is implemented as a bus-powered, full speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

### 2.1 Block Diagram





## 3.0 Power Switch Feature

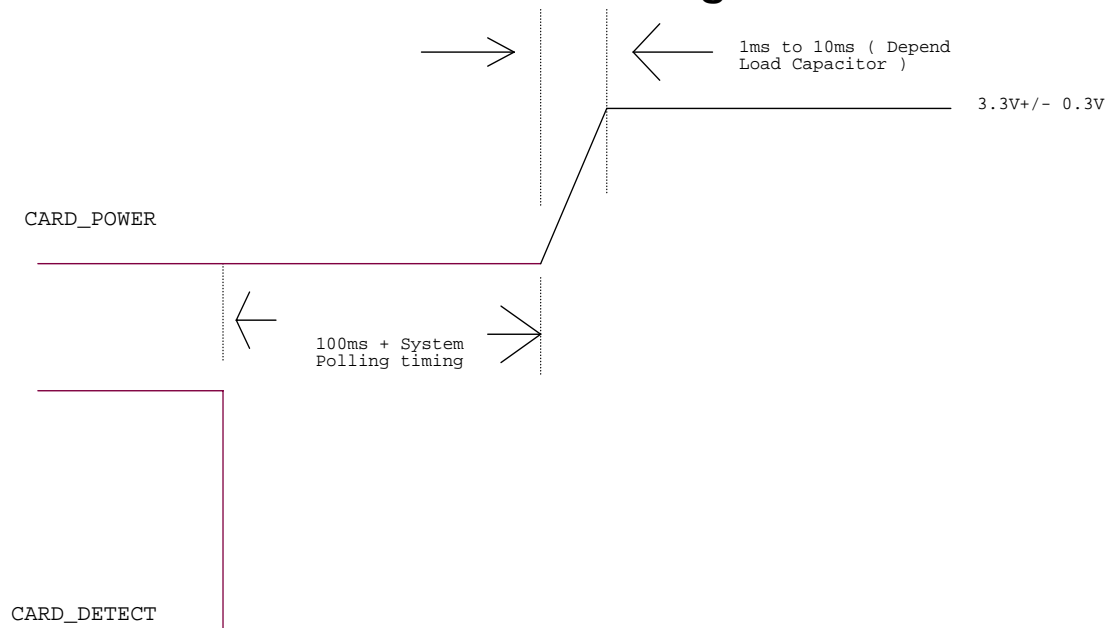
AU6369 integrates a 3.3V to 2.5V voltage regulator and power switch to replace all MOS chips for flash card power supply.

### 3.1 Card Power Output Current Range

- For MS/SD
  - ◆ MAX: 100mA
  
- For XD/SMC
  - ◆ MAX: 70mA
  
- Card power output voltage range
  - ◆ MS/XD/SD/SMC:  $3.3V \pm 0.3V$

1.1. AU6369 will turn off all of Card Power in suspend mode

### 3.2 Card Detect Power-on Timing





# 4.0 Pin Assignment

The AU6369 is packed in 48pin-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

Figure 4.1 Pin Assignment Diagram

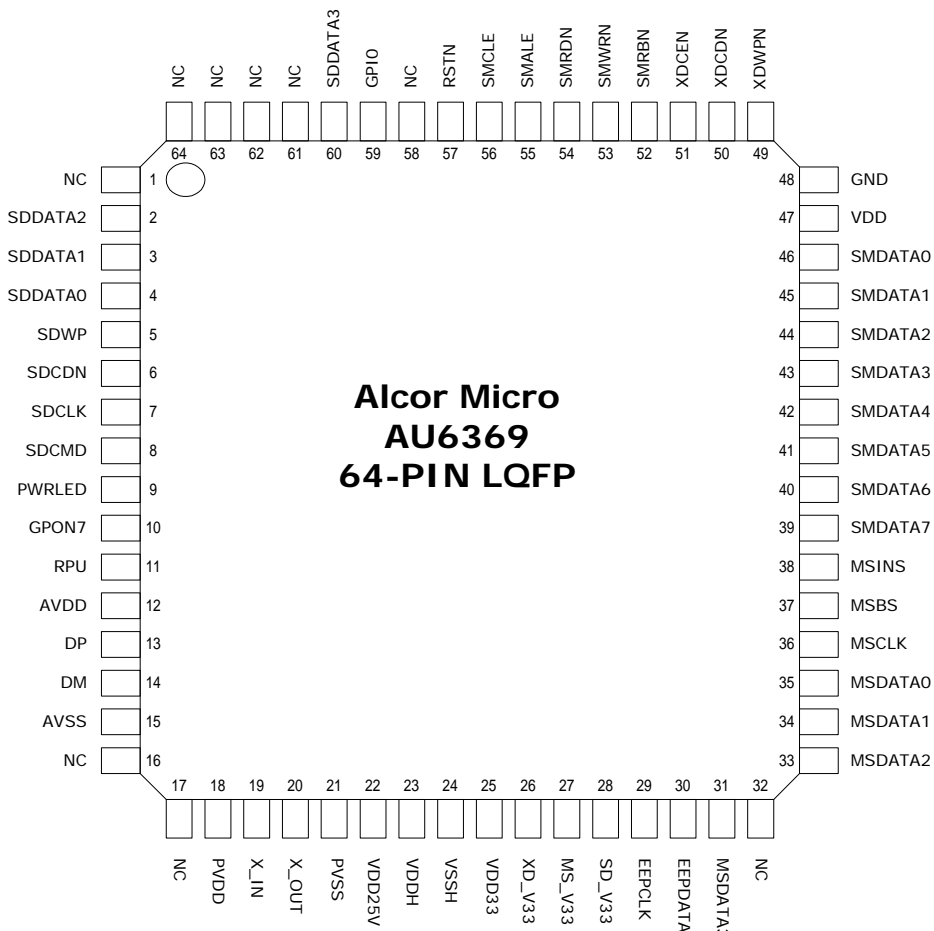




Table 4.1 Pin Descriptions

Pin #	Pin Name	I/O	Description
1	NC		
2	SDDATA2	I/O	SD Data2
3	SDDATA1	I/O	SD Data1
4	SDDATA0	I/O	SD Data0
5	SDWP	I	SD Write Protect
6	SDCDN	I	SD Card Detect
7	SDCLK	O	SD CLK
8	SDCMD	I/O	SD CMD
9	PWRLED	O	Power LED; (Normal:"0"; Suspend"1")
10	GPON7	O	Card insert LED; (Card inserted:"0";
11	RPU	I	Connected with an 3.9k pull up resistor to 3.3 VDD
12	AVDD	I	Analog Power 3.3V
13	DP	I/O	USB DP
14	DM	I/O	USB DM
15	AVSS	PWR	Analog Ground
16	NC		
17	NC		
18	PVDD	I	OSC Power 3.3V
19	X_IN	I	12 MHz crystal input.
20	X_OUT	O	12 MHz crystal output.
21	PVSS	PWR	OSC Ground
22	VDD25V	O	Core Power 2.5V
23	VDDH	I	IO Power 3.3V
24	VSSH	PWR	IO Ground
25	VDD33	I	Switch Power 3.3V
26	XD_V33	O	XD Card Power
27	MS_V33	O	MS Card Power
28	SD_V33	O	SD Card Power
29	EEPCLK	O	EEPROM Clock
30	EEPDATA	I/O	EEPROM Data
31	MSDATA3	I/O	MS Data3
32	NC		
33	MSDATA2	I/O	MS Data2
34	MSDATA1	I/O	MS Data1
35	MSDATA0	I/O	MS Data0
36	MSCLK	O	MS CLK
37	MSBS	O	MS BS
38	MSINS	I	MS Card Detect (Insert:"0"; Extraction:"1";Default:"1")
39	SMDATA7	I/O	SM Data7
40	SMDATA6	I/O	SM Data6
41	SMDATA5	I/O	SM Data5
42	SMDATA4	I/O	SM Data4

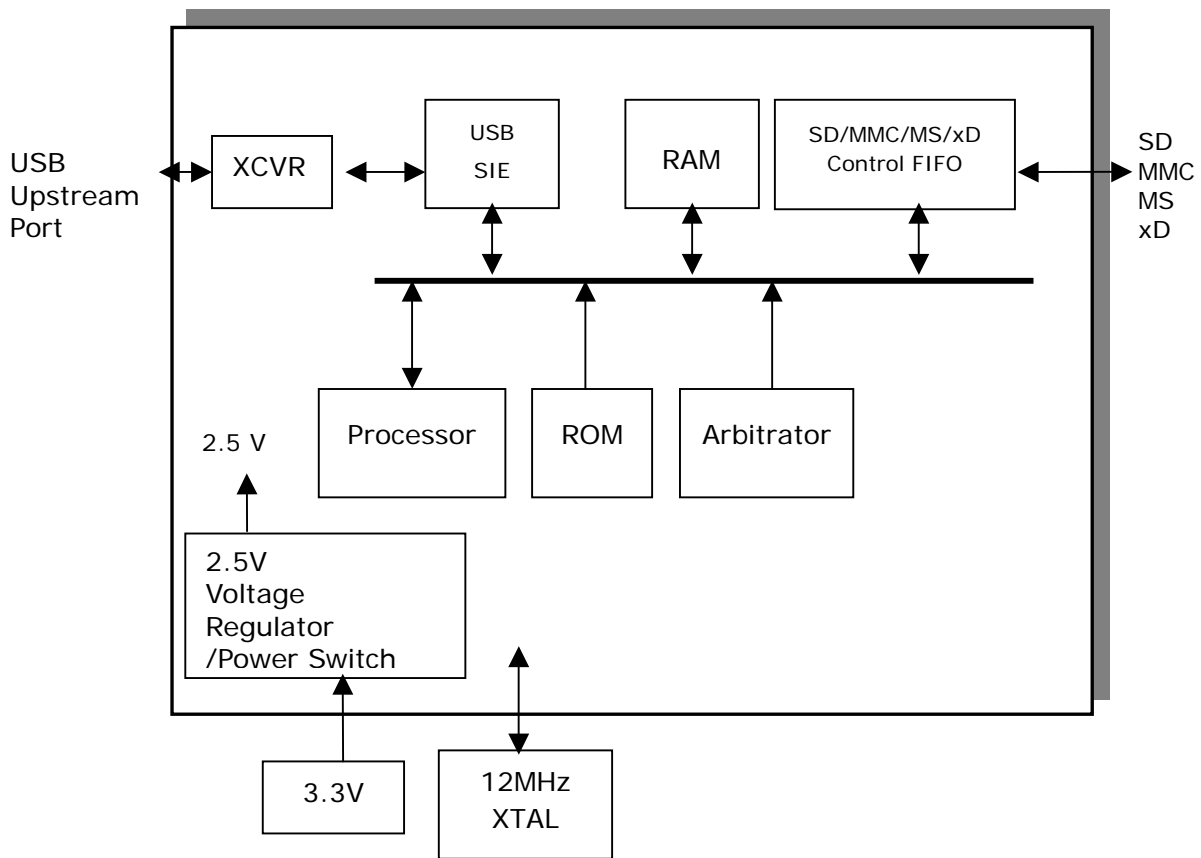


43	SMDATA3	I/O	SM Data3
44	SMDATA2	I/O	SM Data2
45	SMDATA1	I/O	SM Data1
46	SMDATA0	I/O	SM Data0
47	VDD	I	Core power 2.5V
48	GND	PWR	Core Ground
49	XDWPN	O	XD WP
50	XDCDN	I	XD CD
51	XDCEN	O	XD CE
52	SMRBN	I	External pull up with 470K to 3.3V.
53	SMWRN	O	SM WR
54	SMRDN	O	SM RD
55	SMALE	O	SM ALE
56	SMCLE	O	SM CLE
57	RSTN	I	Chip Reset (Reset:"0"; Normal:"1"), pull up with RC
58	NC		
59	GPIO	I	Slot Mode Select (GPI1, GPIO) = (0,0) : 4.5 Luns (GPI1, GPIO) = (0,1) : 2 Luns (GPI1, GPIO) = (1,0) : 4.5 Luns (GPI1, GPIO) = (1,1) : 1 Lun
60	SDDATA3	I/O	SD Data3
61	NC		
62	NC		
63	NC		
64	NC		

# 5.0 System Architecture and Reference Design

## 5.1 AU6369 Block Diagram

Figure 5.1 AU6369 Block Diagram





## 6.0 Electrical Characteristics

### 6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V <sub>CC</sub>	Power Supply	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>IN</sub>	Input Voltage	-0.3 to 3.3	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>CC</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-40 to 150	°C

### 6.2 Recommended Operating Conditions

Table 6.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V <sub>CC</sub>	Power Supply	3.0	3.3	3.6	V
V <sub>IN</sub>	Input Voltage	0	3.3	5.2	V
T <sub>OPR</sub>	Operating Temperature	-40		115	°C

### 6.3 Leakage Current and Capacitance

Table 6.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I <sub>IN</sub>	Input current	no pull-up or pull-down	-10	±1	10	μA
I <sub>OZ</sub>	Tri-state leakage current		-10	±1	10	μA
C <sub>IN</sub>	Input capacitance	Pad Limit		2.8		pF
C <sub>OUT</sub>	Output capacitance	Pad Limit		2.8		pF
C <sub>BID</sub>	Bi-directional buffer capacitance	Pad Limit		2.8		pF



## 6.4 DC Electrical Characteristics of 3.3V I/O Cells

**Table 6.4 DC Electrical Characteristics of 3.3V I/O Cells**

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
$V_{CC}$	Power supply	3.3V I/O	3.0	3.3	3.6	V
$V_{il}$	Input low voltage	LVTTTL			0.8	V
$V_{ih}$	Input high voltage		2.0			V
$V_{ol}$	Output low voltage	$I_{ol} = 2 \sim 16mA$			0.4	V
$V_{oh}$	Output high voltage	$I_{oh} = 2 \sim 16mA$	2.4			V
$R_{pu}$	Input pull-up resistance	PU=high, PD=low	40	75	190	K
$R_{pd}$	Input pull-down resistance	PU=low, PD=high	40	75	190	K
$I_{in}$	Input leakage current	$V_{in} = V_{CC}$ or 0	-10	$\pm 1$	10	$\mu A$
$I_{oz}$	Tri-state output leakage current		-10	$\pm 1$	10	$\mu A$



## 6.5 USB Transceiver Characteristics

**Table 6.5 Electrical characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AVCC	Analog supply current		3.0	3.3	3.6	V
VCC	Digital supply current		2.25	2.5	2.75	V
I <sub>CC</sub>	Operating supply current	High speed operating at 480 MHz			73	mA
I <sub>CC(susp)</sub>	Suspend supply current	In suspend mode, current with 1.5k pull-up resistor on pin RPU disconnected			120	μA

**Table 6.6 Static characteristic : Digital pin**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V <sub>IL</sub>	Low-level input voltage				0.8	V
V <sub>IH</sub>	High-level input voltage		2.0			V
Output levels						
V <sub>OL</sub>	Low-level output voltage				0.2	V
V <sub>OH</sub>	High-level output voltage		VCC-0.2			V

**AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0 ~115**



**Table 6.7 Static characteristic : Analog I/O pins ( DP/DM )**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver ( HS )						
Input Levels ( differential receiver )						
$V_{HSDIFF}$	High speed differential input sensitivity	$V_{I(DP)} - V_{I(DM)}$ measured at the connection as application circuit	300			mV
$V_{HSCM}$	High speed data signaling common mode voltage range		-50		500	mV
$V_{HSSQ}$	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
$V_{HSDSC}$	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
$V_{HSOI}$	High speed idle level output voltage(differential)		-10		10	mV
$V_{HSOL}$	High speed low level output voltage(differential)		-10		10	mV
$V_{HSOH}$	High speed high level output voltage(differential)		-360		400	mV
$V_{CHIRPJ}$	Chirp-J output voltage ( differential )		700		1100	mV
$V_{CHIRPK}$	Chirp-K output voltage ( differential )		-900		-500	mV
Resistance						
$R_{DRV}$	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
$V_{TERM}$	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver ( FS/LS )						
Input Levels ( differential receiver )						
$V_{DI}$	Differential input sensitivity	$V_{I(DP)} - V_{I(DM)}$	0.2			V
$V_{CM}$	Differential common mode voltage		0.8		2.5	V
Input Levels ( single-ended receivers )						



$V_{SE}$	Single ended receiver threshold		0.8		2.0	V
Output levels						
$V_{OL}$	Low-level output voltage		0		0.3	V
$V_{OH}$	High-level output voltage		2.8		3.6	V

**AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0 ~115**

**Table 6.8 Dynamic characteristic : Analog I/O pins (DP/DM)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
$t_{HSR}$	High-speed differential rise time		500			ps
$t_{HSF}$	High-speed differential fall time		500			ps
Full-Speed Mode						
$t_{FR}$	Rise time	CL=50pF ; 10 to 90 % of $V_{OH}-V_{OL}$ ;	4		20	ns
$t_{FF}$	Fall time	CL=50pF ; 90 to 10 % of $V_{OH}-V_{OL}$ ;	4		20	ns
$t_{FRMA}$	Differential rise/fall time matching ( $t_{FR} / t_{FF}$ )	Excluding the first transition from idle mode	90		110	%
$V_{CRS}$	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
$t_{LR}$	Rise time	CL=200pF-600pF ; 10 to 90 % of $V_{OH}-V_{OL}$ ;	75		300	ns
$t_{LF}$	Fall time	CL=200pF-600pF ; 90 to 10 % of $V_{OH}-V_{OL}$ ;	75		300	ns
$t_{LRMA}$	Differential rise/fall time matching ( $t_{LR} / t_{LF}$ )	Excluding the first transition from idle mode	80		125	%
$V_{CRS}$	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
$V_{OH}$	High-level output voltage		2.8		3.6	V





## 8.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

<b>SIE</b>	Serial Interface Engine
<b>SMC</b>	SmartMedia Card
<b>MS</b>	Memory Stick
<b>SD</b>	Secure Digital
<b>MMC</b>	Multimedia Card
<b>UTMI</b>	USB Transceiver Macrocell Interface



**【MEMO】**

### **About Alcor Micro, Corp**

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader...etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

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